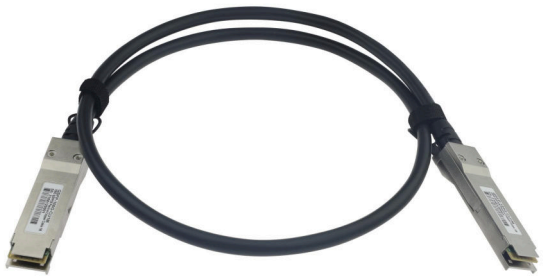
# 100G QSFP28 Direct Attach Passive Copper Cables

# RQS-DAC100G-CU*M

## Product Description

The 100G QSFP28 passive cable assembly products, based on 4 x25G or 4 x28G structure, the product can well satisfy the next generation 100G switches, servers, routers and other products of application requirements.QSFP28 cable adopts optimized design to reduce crosstalk and insertion loss, excellent signal integrity, fully conforms to the next generation 100G Ethernet and Infiniband EDR standards.



100G QSFP28 DAC

## Features

- 4-channel full-duplex passive copper cable
- Data rate up to 100Gbps (4x 25Gbps)
- SFF-8665 compliant QSFP28 connectors
- SFF-8636 compliant I2C management interface
- IEEE 802.3bj 100GBASE-CR4 compliant
- Copper link length up to 5m (passive limiting)
- Hot Pluggable
- Low power consumption
- Excellent signal integrity, low insertion loss and low crosstalk
- Operating case temperature range: 0°C to +70°C
- Single 3.3V supply voltage
- RoHS compliant

## Application

- 100G Ethernet 100GBASE-CR4
- InfiniBand 4x EDR
- SAS, servers, hubs, switches and routers
- Data Center

## Recommended Operating Conditions

| Parameter | Symbol | Min | Typical | Max | Unit |
|---|---|---|---|---|---|
| Storage Ambient Temperature | | -40 | | +85 | °C |
| Operating Case Temperature | Tc | 0 | | +70 | °C |
| Power Supply Voltage | VCC3 | 3.14 | 3.3 | 3.47 | V |
| Data Rate Per Lane | | 1 | | 25.78 | Gb/s |

## High Speed Characteristics

| Parameter | Symbo | Min | Typical | Max | Uni | Note |
|---|---|---|---|---|---|---|
| Differential Impedance | RIN,P- | 90 | | 110 | Ω | |
| Insertion loss | SDD21 | | | 22.48 | dB | At 12.8906 GHz |
| Differential Return Loss | SDD11 | | | See 1 | dB | At 0.05 to 4.1 GHz |
| | SDD22 | | | See 2 | dB | At 4.1 to 19 GHz |
| Common-mode to common-mode output return loss | SCC11 | 2 | | | dB | At 0.2 to 19 GHz |
| | SCC22 | | | | | |
| Differential to common-mode return loss | SCD11 | | | See 3 | dB | At 0.01 to 12.89 |
| | SCD22 | | | See 4 | | At 12.89 to 19 GHz |
| Differential to common Mode Conversion Loss | SCD21 | | | 10 | dB | At 0.01 to 12.89 |
| | | | | See 5 | | At 12.89 to 15.7 |
| | | | | 6.3 | | At 15.7 to 19 GHz |
| Channel Operating Margin | COM | 3 | | | dB | |

Notes:

1.Reflection Coefficient given by equation SDD11(dB) < 16.5 - 2 × SQRT(f ), with f in GHz

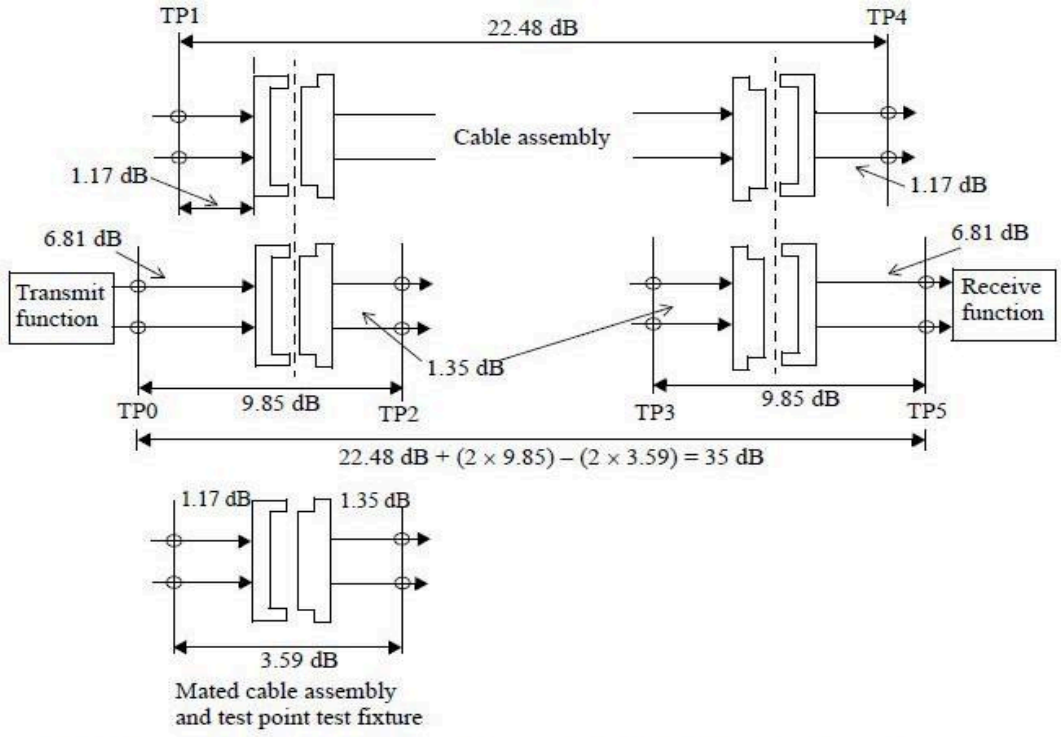
2.Reflection Coefficient given by equation SDD11(dB) < 10.66 - 14 × log10(f/5.5), with f in GHz

3.Reflection Coefficient given by equation SCD11(dB) < 22 - (20/25.78)*f, with f in GHz

4.Reflection Coefficient given by equation SCD11(dB) < 15 - (6/25.78)*f, with f in GHz

5.Reflection Coefficient given by equation SCD21(dB) < 27 - (29/22)*f, with f in GHz

## Channel insertion loss budget




NOTE—The connector insertion loss is 1.07 dB for the mated test fixture. The host connector is allocated 0.62 dB of additional margin.

**Figure 92A–2—35 dB channel insertion loss b[illegible] 12.8906 GHz**

## Pin Descriptions

| PIN | Logic | Symbol | Name/Description | Note |
|---|---|---|---|---|
| 1 | | GND | Ground | 1 |
| 2 | CML-I | Tx2n | Transmitter Inverted Data Input | |
| 3 | CML-I | Tx2p | Transmitter Non-Inverted Data Input | |
| 4 | | GND | Ground | 1 |
| 5 | CML-I | Tx4n | Transmitter Inverted Data Input | |
| 6 | CML-I | Tx4p | Transmitter Non-Inverted Data Input | |
| 7 | | GND | Ground | 1 |
| 8 | LVTTL-I | ModSelL | Module Select | |
| 9 | LVTTL-I | ResetL | Module Reset | |
| 10 | | Vcc Rx | +3.3V Power Supply Receiver | 2 |
| 11 | LVCMSI/O | SCL | 2-wire serial interface clock | |
| 12 | LVCMOSI/O | SDA | 2-wire serial interface data | |
| 13 | | GND | Ground | 1 |
| 14 | CML-O | Rx3p | Receiver Non-Inverted Data Output | |
| 15 | CML-O | Rx3n | Receiver Inverted Data Output | |
| 16 | | GND | Ground | 1 |
| 17 | CML-O | Rx1p | Receiver Non-Inverted Data Output | |
| 18 | CML-O | Rx1n | Receiver Inverted Data Output | |
| 19 | | GND | Ground | 1 |
| 20 | | GND | Ground | 1 |
| 21 | CML-O | Rx2n | Receiver Inverted Data Output | |
| 22 | CML-O | Rx2p | Receiver Non-Inverted Data Output | |
| 23 | | GND | Ground | 1 |
| 24 | CML-O | Rx4n | Receiver Inverted Data Output | |
| 25 | CML-O | Rx4p | Receiver Non-Inverted Data Output | |
| 26 | | GND | Ground | 1 |
| 27 | LVTTL-O | ModPrsL | Module Present | |
| 28 | LVTTL-O | IntL | Interrupt | |
| 29 | | Vcc Tx | +3.3V Power supply transmitter | 2 |
| 30 | | Vcc1 | +3.3V Power supply | 2 |
| 31 | LVTTL-I | LPMode | Low Power Mode | |
| 32 | | GND | Ground | 1 |
| 33 | CML-I | Tx3p | Transmitter Non-Inverted Data Input | |
| 34 | CML-I | Tx3n | Transmitter Inverted Data Input | |

Note 1: GND is the symbol for signal and supply (power) common for the QSFP+ module. All are common within the QSFP+ module and all module voltages are referenced to this potential unless otherwise noted. Connect these directly to the host board signal-common ground plane.

Note 2: Vcc Rx, Vcc1 and Vcc Tx are the receiver and transmitter power supplies and shall be applied concurrently. Requirements defined for the host side of the Host Edge Card Connector are listed in Table 6. Recommended host board power supply filtering is shown in Figure 4. Vcc Rx Vcc1 and Vcc Tx may be internally connected within the QSFP+ module in any combination. The connector pins are each rated for a maximum current of 500mA.

## Mechanical Dimensions